# An Ultra Low Noise W-Band Monolithic Three-Stage Amplifier Using 0.1 $\mu m$ Pseudomorphic InGaAs/GaAs HEMT Technology

H. Wang, T. N. Ton, K. L. Tan, G. S. Dow, T. H. Chen, K. W. Chang, J. Berenz, B. Allen, P. Liu, D. Streit, G. Hayashibara and L. C. T. Liu

TRW
Electronics & Technology Division
One Space Park, Redondo Beach, CA 90278

## ABSTRACT

An ultra low noise W-band monolithic three-stage amplifier based on 0.1 $\mu m$ pseudomorphic InGaAs/GaAs HEMT devices has been developed. This amplifier has a measured noise figure of 3.5 dB with an associated small signal gain of 21 dB at 94 GHz. This is the best reported performance of a monolithic W-band high gain LNA and shows significant improvement compared with previous records in terms of noise figure and associated gain. The success of this LNA development is attributed to the excellent device performance and a rigorous design/analysis methodology. The state-of-the-art MMIC performance shows great promise of the emerging technology for low cost W-band receiver applications.

## INTRODUCTION

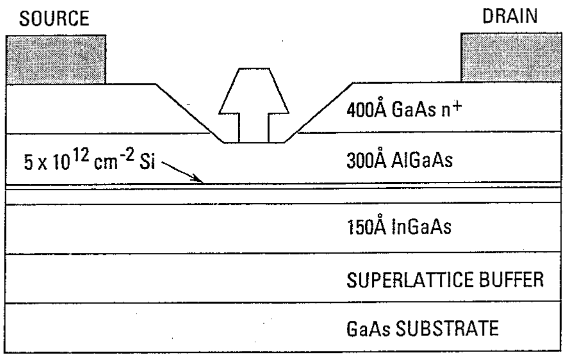
Monolithic millimeter-wave integrated circuits provide significant advantages of small size, repeatability and low cost at high volume over the conventional hybrid integrated circuit components for millimeter wave radar, electronic warfare, smart weapon, and radiometric system applications. The low noise amplifier (LNA) is a key component in the receiving chain of these systems. The motivation of this work was achieving state-of-the-art performance of a monolithic LNA in W-band to improve the performance of existing systems and enable new applications.

Both GaAs and InP based high electron mobility transistors (HEMTs) have demonstrated good gain and noise performance in W-band [10]-[13]. Although the InP based discrete HEMTs show better performance at W-band or higher frequencies [10]-[14], the maturity of MMIC fabrication using GaAs based HEMT technology is more advanced than using InP based HEMT technology. In fact, no comparable state-of-the-art W-band monolithic InP-based LNAs have been reported to date. A W-band monolithic three-stage LNA based on 0.1 $\mu m$ pseudomorphic (PM) InGaAs/GaAs HEMT technology has been designed, fabricated and tested. The LNA chip has demonstrated superior performance: 21 dB gain and 3.5 dB noise figure at 94 GHz without any tuning. The highest gain of W-band monolithic LNA reported before was a four-stage design which showed 23 dB gain [8]. However, the operating frequency and noise figure were not clearly indicated. The best noise figure of a 94 GHz monolithic LNA achieved previously was a one-stage design with 3.5 dB noise figure [9]. The results reported in this paper not only are the best multi-stage monolithic LNA performance at W-band frequency at present time [1]-[9], but also rival the recently reported hybrid LNA results [10]-[13] using both PM and lattice-matched HEMTs. Accurate modeling techniques were essential to the success of this monolithic circuit design, which included active device and full-wave electromagnetic (EM) analysis of passive matching structures.

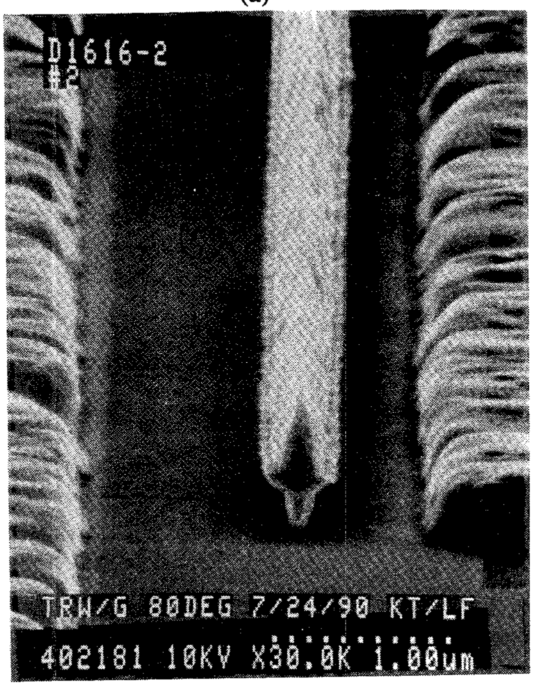
X

## DEVICE CHARACTERISTICS AND MODELING

The devices reported in this paper have been optimized for high gain operation at W-band. The 22% PM InGaAs HEMT uses planar doping to achieve high channel aspect ratio as well as higher electron transfer efficiency. The MMIC fabrication process used for this work has been previously reported [13]. A cross-section and the SEM photograph for the gate area of the HEMT device are shown in Fig. 1. The 0.1 $\mu m$ T-gate PM InGaAs HEMTs fabricated using this process typically have a transconductance of 670 $mS/mm$ with an $f_t$ as high as 140 GHz. The discrete HEMT device DC yield in process control monitors (PCMs) on this 3" diameter GaAs wafer is 83%. This process has demonstrated excellent yield and reproducibility over the past




(a)




(b)

Fig. 1. (a) The profile and (b) the SEM photograph for the gate area of the 0.1 $\mu m$ PM InGaAs/GaAs HEMT device.

two years and is presently transferred to production in our manufacturing process line.

The HEMT linear small signal equivalent circuit parameters are obtained from careful fit of the measured small signal $S$-parameters to 40 GHz. Noise model parameters used for simulation are obtained from fitting measured noise parameters to 26 GHz. These parameters are consistent with an estimation based on device physical dimensions and parameters. A set of specially designed on-wafer calibration standards consisting of co-planar wave-guide (CPW) open, short, load and through which have the same feed patterns as the device to be tested are modeled carefully via a full-wave EM analysis [15]. The measurement accuracy can be ensured by using these calibration patterns, thus improves the accuracy of the frequency extrapolation model to W-band. The details of this modeling procedure was documented in [2].

## MONOLITHIC CIRCUIT DESIGN

Fig. 2 shows a photograph of the complete monolithic three-stage LNA with the chip dimensions of 3.2 × 1.2 $mm^2$. Each stage utilizes a 40 $\mu m$ HEMT with four gate fingers. The circuit is designed for low noise figure based on reactive matching technique. The matching networks are quasi-low pass filter structures and realized by cascade high-low impedance microstrip lines on 100 $\mu m$ thick GaAs substrate. Edge coupled lines are used for DC block and radial stubs are employed for RF by pass. $N^+$ bulk resistors are used to ensure bias network stability, and reactive ion etching (RIE) process is used to fabricate back side via holes for grounding.

A design procedure using full-wave EM analysis [15] for the passive structures to eliminate the uncertainties due to quasi-static models was incorporated with the W-band monolithic LNA development. The design methodology was also described in [2].

## MEASUREMENT RESULTS

The three-stage monolithic LNA were measured in a WR10 waveguide test fixture. Antipodal finline transitions on 125 $\mu m$ thick fused silica substrate are used to couple the signal from waveguide to microstrip. The insertion loss of this transition fixture with a back-to-back transi-

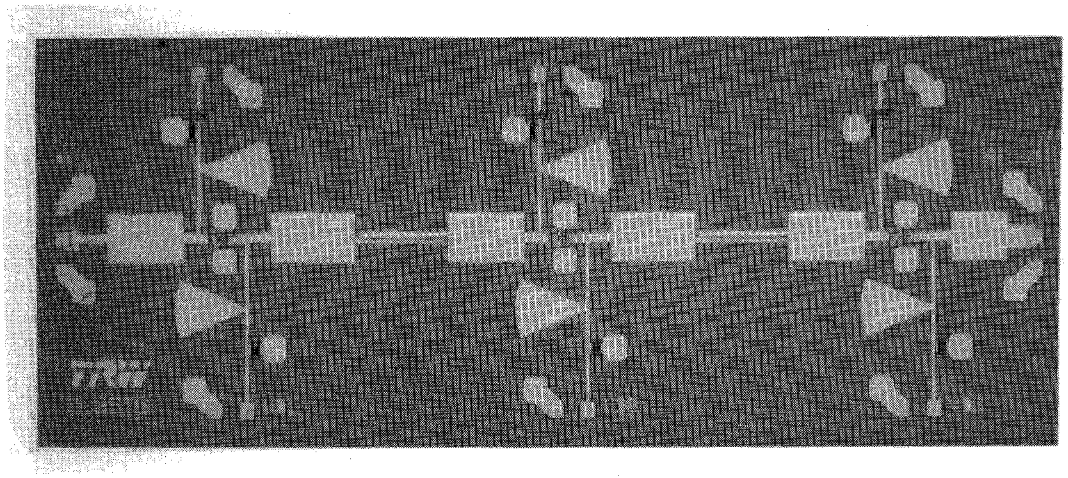


Fig. 2. Photograph of the W-band three-stage MMIC LNA.

tion connection is 1.4 dB from 91 to 97 GHz as shown in Fig. 3. The measurement results of the LNA described below were corrected assuming half the back-to-back insertion loss (0.7 dB) is attributable separately to the input and output of the circuit under test.

The measurement data from 91 to 97 GHz are presented in Fig. 4. Noise figure is better than 4 dB and the associated small signal gain greater than 20 dB across the band. At 94 GHz, it demonstrates 21 dB gain and 3.5 dB noise figure. The noise and gain variation are within 0.5 and 2 dB across the band, respectively. The data was taken under the bias condition at a drain voltage of 2.5*V* and a gate voltage of 0*V* for each stage. Another chip on the same wafer was also measured. The noise figure is similar to that of the first chip but the associated gain is 1 dB lower. The improvement of noise performance compared to previously published results [2],[9] is due to the improved noise match. The success of this second design iteration also shows the reproducibility of the MMIC process.

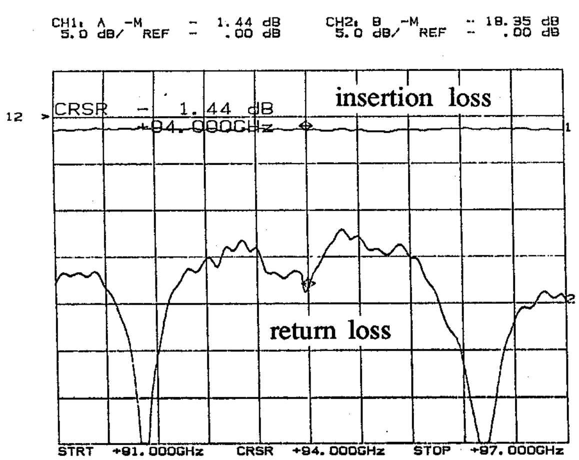



Fig. 3. Measured insertion and return loss of the finline transition.

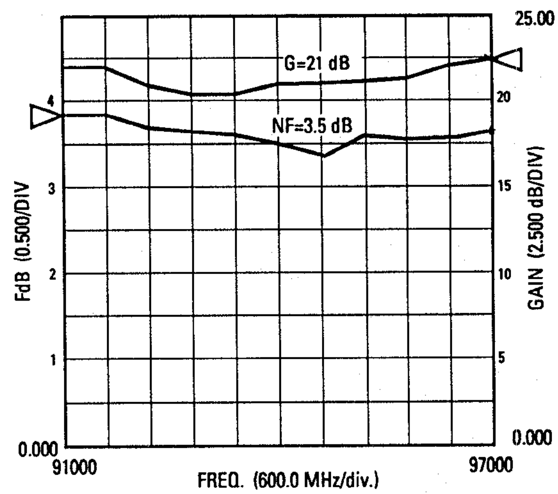



Fig. 4. Measured results of the W-band three-stage MMIC LNA, including noise figure and associated small signal gain from 91 to 97 GHz.

## SUMMARY

We have demonstrated a W-band monolithic three-stage LNA with state-of-the-art performance. At 94 GHz, a small signal gain of 21 dB and a noise figure of 3.5 dB was achieved. The excellent device characteristics together with the high yield capability and rigorous design/analysis methodology are the foundations of this successful MMIC development. The superior results of this monolithic LNA also enable many system applications at this frequency, such as smart munition and radiometers.

## ACKNOWLEDGMENT

This work is done under TRW internal R&D funds. The authors would like to thank J. Coakley and J. Yonaki for the layout effort, J. J. Raggio for the device testing, R. Dia for wafer processing, the MBE and EBL groups in TRW for their excellent help and MIMIC Phase 2 Program for the support of chip testing.

## REFERENCES

[1] H. Wang et al., "A high performance W-band monolithic InGaAs pseudomorphic LNA," *1991 IEEE MTT-S International Microwave Symposium Digest,* vol. 3, pp. 943-946, June, 1991.

[2] H. Wang et al., "High performance W-band monolithic InGaAs pseudomorphic LNAs and design/analysis methodology," *IEEE Trans. on Microwave Theory Tech, March, 1992.*

[3] N. Camilleri, P. Chye, P. Gregory and A. Lee, "A W-band monolithic amplifier," *1990 IEEE MTT-S International Microwave Symposium Digest,* vol. 2, pp. 903-906, May, 1990.

[4] H. B. Sequeira et al., "Monolithic GaAs W-band pseudomorphic MODFET amplifiers," *1990 IEEE GaAs IC Symposium Digest,* pp. 161-164, Nov., 1990.

[5] R. Majidi-Ahy et al. "100 GHz high-gain InP MMIC cascode amplifier," *1990 IEEE GaAs IC Symposium Digest,* pp. 173-176, Nov., 1990.

[6] R. Majidi-Ahy et al., "94 GHz InP MMIC five-section distributed amplifier," *Elect. Lett.,* vol. 26, no. 2, pp. 91-92, Jan., 1990

[7] R. Majidi-Ahy et al., "5-100 GHz InP CPW MMIC 7-section distributed amplifier," *IEEE 1990 Microwave and Millimeter-wave Monolithic Circuits Symposium Digest,* pp. 31-34, May, 1990.

[8] M. W. Trippe et al., "Millimeter-wave MMIC receiver components," *IEEE 1991 Microwave and Millimeter-wave Monolithic Circuits Symposium Digest,* pp. 51-54, June, 1991.

[9] H. Wang et al., "State-of-the-art low noise performance of 94 GHz monolithic amplifiers using 0.1 $\mu m$ InGaAs/GaAs pseudomorphic HEMT technology," *IEEE International Electronic Device Meeting Digest,* pp. 939-942, Washington D. C., Dec., 1991.

[10] K. H. G. Duh et al., "W-band InGaAs HEMT low noise amplifiers," *1990 IEEE MTT-S International Microwave Symposium Digest,* vol. 1, pp. 595-598, May, 1990.

[11] K. H. G. Duh et al, "A super low-noise 0.1 $\mu m$ T-gate InAlAs-InGaAs-InP HEMT," *IEEE Microwave and Guided Wave Letters,* vol. 1, no. 5., pp. 114-116, May, 1991.

[12] P. D. Chow et al., "Ultra low noise high gain W-band InP-based HEMT downconverter," *1991 IEEE MTT-S International Microwave Symposium Digest,* vol. 3, pp. 1041-1044, June, 1991.

[13] K. L. Tan et al, "94 GHz 0.1 $\mu m$ T-gate low noise pseudomorphic InGaAs HEMTs," *IEEE Electronic Device Letters,* vol. 11, no. 12., pp. 585-587, Dec., 1990.

[14] K. L. Tan et al., "140 GHz 0.1 $\mu m$ gate-length pseudomorphic $In_{0.52}Al_{0.48}As/In_{0.60}Ga_{0.40}As/InP$ HEMT," *IEEE International Electronic Device Meeting Digest,* Washington D. C., Dec., 1991.

[15] J. C. Rautio and R. F. Harrington, "An electromagnetic time-harmonic analysis of shielded microstrip circuits," *IEEE Trans. on Microwave Theory Tech.,* vol. 35, pp. 726-730, Aug., 1987.